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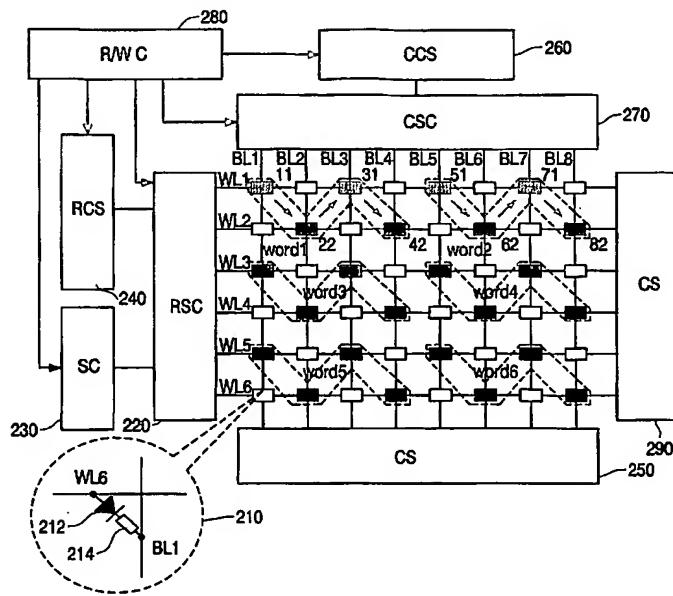
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(54) Title: **SIMULTANEOUS READING FROM AND WRITING TO DIFFERENT MEMORY CELLS**



WO 2004/084226 A1

(57) Abstract: A nonvolatile memory array includes a grid of word lines WL1,...,WL6 and bit lines BL1,...,BL8. Of a plurality of memory cells 210, each memory cell is located at an intersection region of one of the word lines and one of the bit lines. A read/write circuit 280 for reading/writing a data word including a plurality of bits is operative to map each pair of sequential bits of the data word to a respective pair of memory cells located at intersection regions of both a different word line and a different bit line.



PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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